DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First embodiment Figure 1 is a circuit diagram showing the first embodiment of the drive circuit of this invention. Figure 1 shows the arrangement of the source drivers that comprise the drive circuit of the first embodiment of this invention and the wiring method of the data bus that supplies signals to the source drivers. Also shown in Figure 1 is part of the drive circuit consisting of source drivers 100-1, 100-2, 100-3. In each source driver, for example, digital signals are supplied by six input signal lines. Omitted from the diagram are signal lines that transmit drive signals from each source driver to the LCD panel. An actual drive circuit will have, for example, about 6-12 source drivers, and connected to each source driver are, besides the six digital signal lines that supply digital signals, a clock signal line and control signal lines that supply a clock signal and other control signals, as well as about 100-400 signal lines that are driven by the source drivers. Figure 2 shows an example of the composition of a source driver that constitutes the drive circuit of this embodiment. Since each source driver 100-1, 100-2, 100-3 that makes up the drive circuit shown in Figure 1 has the same composition, in Figure 2, without loss of generality, a source driver that makes up the drive circuit of this embodiment is denoted labeled with the symbol 100. Source driver 100 that constitutes the drive circuit of this embodiment is formed by sealing with resin a silicon substrate (semiconductor chip) 110 on the surface of a flexible wiring board. Formed on the surface of the flexible wiring board are input pad unit 130 and output pad unit 140, which are made of a metal film having the prescribed pattern, lines 132 between input pad unit 130 and the input terminals of silicon substrate 110, and lines 142 between the output terminals of silicon substrate 110 and output pad unit 140. Drive signals that drive the LCD panel are generated by an integrated circuit (IC) formed on the silicon substrate in accordance with digital signals input from input pad unit 130 and clock signals and other control signals, and the drive signals are supplied to the LCD panel via lines 142 and output pad unit 140. Switch unit 120 and processing unit 122 are provided on the integrated circuit formed on silicon substrate 110. In accordance with switching control signal Sw, which is input via input pad 150, switch unit 120 converts the signals input from input terminals i1', i2', ..., i6' into the prescribed lineup sequence

and outputs them to output terminals i1, i2, ..., i6, respectively. Also, output terminals i1, i2, ..., i6 of switch unit 120 are connected to input terminals j1, j2, ..., j6 of processing unit 122, respectively. Figure 3 is a diagram that shows the principle of operation of switch unit 120, showing the connection relationship between the input terminals i1', i2', ..., i6' of switch unit 120 and output terminals i1, i2, ..., i6 when switching control signal Sw is at low level "L" and high level "H". As shown in the diagram, when switching control signal Sw is at low level "L", the signal input to terminal i1' is output to output terminal i1, the signal input to terminal i2' is output to output terminal i2, ..., and the signal input to terminal i6' is output to output terminal i6. And when switching control signal Sw is at high level "H", the lineup sequence of the signals input to input terminals i1', i2', ..., i6' is reversed by switch unit 120 and is output to output terminals i1, i2, ..., i6. For example, the signal input to terminal i1' is output to output terminal i6, the signal input to terminal i2' is output to output terminal i5, and the signal input to terminal i6' is output to output terminal i1. As stated above, switch unit 120 is provided on source driver 100, and the signals input to input terminals i1', i2', .., i6' are rearranged and supplied to input terminals i1, i2, .., i6 of processing unit 122 according to switching control signal Sw input from outside. If the drive circuit is put together using multiple source drivers 100 shown in Figure 2, then for example switching control signals Sw of different levels are input to the odd-numbered and even-numbered source drivers, respectively. In this way, the signal lines of data bus 200 can be wired as shown in Figure 1. That is, the signal lines of data bus 200 into which digital signals D1, D2, ..., D6 can be wired in a "one-stroke-of-the-pen" wiring pattern, in which they are arranged parallel to each other without intersecting each other. As shown in Figure 1, a switching control signal Sw that has a low level, for example, the level of the ground electric potential GND, is input to first source driver 100-1, a switching control signal Sw of high level, for example, the level of the power source voltage VDD, is input to second source driver 100-2, and a low-level switching control signal Sw is input to third source driver 100-3. That is, a low-level switching control signal Sw is input to the odd-numbered source drivers, and a high-level switching control signal Sw is input to the even-numbered source drivers. In odd-numbered source driver 100-1 or 100-3, the signal lines of the data bus that supplies digital signals D1, D2, ..., D6 are connected to pads

I1, I2, ..., I6, respectively. Because a low-level switching signal Sw is input to source drivers 100-1 and 100-3, the digital signals input to pads I1, I2, ..., I6 are output by switch unit 120 to its output terminals i1, i2, ..., i6. On the other hand, in even-numbered source driver 100-2, the signal lines of the data bus that supplies digital signals D1, D2, ..., D6 are connected to pads I6, I5, ..., I1, respectively. Because a high-level switching signal Sw is input to source drivers 100-2, the digital signals input to input pads I6, I5, .., I1 are rearranged by switch unit 120 and output to its output terminals i1, i2, ..., i6. Thus, in the wiring pattern of data bus 200 shown in Figure 1, by virtue of the fact that different switching control signals Sw are supplied to the odd-numbered and even-numbered source drivers, digital signals D1, D2, ..., D6 are input in correct sequence to the input terminals i1, i2, ..., i6 of the processing unit of each source driver. Figure 4 is a block diagram showing part of a liquid-crystal display device composed of the drive circuit and LCD panel of this embodiment. Figure 4(a) is a plan view of the liquid-crystal display device, and Figure 4(b) is a cross-sectional view of the liquid-crystal display device. As shown here, the liquid-crystal display device consists of control circuit 210 formed on substrate 220, multiple source drivers 100-1, 100-2, ..., 100-m of TCP structure, and LCD panel display 240. Formed on substrate 220 are, besides control circuit 210, data bus ~~220~~ 200, which transmits digital signals to source drivers 100-1, 100-2, ..., 100-m, and data bus terminal resistance 260. The cross-sectional view of Figure 4(b) is a cross-sectional view along line ~~A-A'~~ 4B-4B in Figure 4(a). As shown here, source driver 100-i (where i = 1, 2, ..., m) consists of flexible wiring board 112 and silicon substrate 110, which is sealed by resin on said flexible wiring board 112. On the surface of flexible wiring board 112 are input and output pads and wiring formed by metal film formed in the prescribed patterns, and digital signals transmitted by data bus 200 are input via the input pads and wiring formed on the flexible wiring board to the integrated circuit formed on the silicon substrate. The digital signals that are input are rearranged by switch unit 120 of the integrated circuit according to switching control signal Sw and are input to processing unit 122. In processing unit 122, signals are generated that drive LCD panel 240 according to the digital signals and the other control signals that are input. The drive signals are input to the respective signal lines of LCD panel 240 via the wiring and output pads formed on the flexible wiring board. Also, although not shown in Figure

4(a), the signal lines of data bus 200 wired on substrate 220 are wired in a one-stroke-of-the-pen wiring pattern in which they are arranged parallel to each other without intersecting each other as shown in Figure 1, so in substrate 220 data bus 200 can be formed by one-layer wiring. In addition, wiring length Lsb from data bus 200 to the silicon substrate of the source driver is approximately determined by the wiring length between the input pads on the flexible wiring board and the input terminals on the silicon substrate, as shown in Figures 1 and 2. Thus said wiring length Lsb is much shorter than in the wiring method in a conventional drive circuit, which can reduce the waveform distortion of the signals supplied to the source driver. That is, the drive circuit and wiring method of this embodiment make it possible to supply high-speed digital signals to the source driver while suppressing waveform distortion of the signals.

Second embodiment Figure 5 is a circuit diagram showing the second embodiment of the drive circuit of this invention. As shown here, the drive circuit of this embodiment consists of source drivers 102-1, 102-2, ..., 102-3 .... The source drivers that comprise the drive circuit of this embodiment, like the source drivers of the first embodiment described above, have a switch unit on the integrated circuit formed on the silicon substrate. Said switch unit arranges digital signals D1, D2, .., D6 input to input pads I11, I21, ..., I61 into the prescribed order according to switching control signal Sw and supplies them to the processing unit. Figure 6 shows an example of the composition of a source driver. Labeled here with symbol 102 is a source driver that comprises the drive circuit of this embodiment. Source driver 102 of this embodiment is formed with, for example, silicon substrate 110 sealed by resin on the surface of a flexible wiring board. Also formed on the surface of the flexible wiring board are input pad unit 130a made of metal film having the prescribed patterns, lines 132a between the input pads and the input terminals of silicon substrate 110, output pad unit 140, and lines 142 between the output pads and silicon substrate 110. According to the digital signals, clock signal, and other control signals input from input pad unit ~~132 [sic; should be 130a?]~~ 103a, an integrated circuit (IC) formed on the silicon substrate generates drive signals that drive the LCD panel, and these drive signals are supplied to the LCD panel via signal lines 142 and output pad unit 140. As shown here, in source driver 102, input

pad unit ~~132 [sic; should be 130a?]~~ 130a consist of multiple sets of pads in pairs. Formed between the two pads in each pair and the input terminal on silicon substrate 110 are two signal lines that are parallel to each other. For example, signal lines are formed between each of pads I11, I12, which form a pair, and input terminal i1' of switch unit 120 on the silicon substrate. In this way, U-shaped wiring is formed between each pad pair and the corresponding input terminal of silicon substrate 110. Digital signals input from the respective pads of pad unit 130a are input to input terminals i1', i2', ..., i6' of switch unit 120. Switch unit 120 rearranges the digital signals input to input terminals i1', i2', ..., i6' according to switching control signal Sw input from input pad 150 and outputs them to output terminals i1, i2, ..., i6. The operation of switch unit 120 is the same as that of the switch unit of the source driver of the first embodiment described above, so in the respective input and output terminals the connection relationship is switched according to switching control signal Sw as shown in Figure 3. Signals output from output terminals i1, i2, ..., i6 of switch unit 120 and the clock signal and other control signals input from pads I71, I81 are input to input terminals j1, j2, .., j7, j8 of processing unit 122, respectively. According to these signals input from the input terminals, processing unit 122 generates drive signals that drive the LCD panel and outputs them to output terminals k1, k2, ..., kn. The drive signals output from output terminals k1, k2, ..., kn are supplied to the LCD panel via lines 142 and output pads O1, O2, ..., On, respectively. As described above, in the drive circuit of this embodiment, switch units are provided on the respective source drivers, said switch units take digital signals that are input, arrange them in the prescribed order according to switching control signal Sw, and input them to the processing unit, so as shown in Figure 5, the signal lines of the data bus that transmit digital signals D1, D2, ..., D6 are arranged in a one-stroke-of-the-pen wiring pattern in which they do not intersect each other, and data bus 200 can be formed with one layer of wiring. Also, with the drive circuit of this embodiment, in each source driver the input pads are constituted in pad pairs, and a signal line is formed between each pad of a pad pair and an input terminal on the silicon substrate, so the signal input from one side of a pad pair is input to the input terminal of the silicon substrate through wiring between its pad and an input terminal on the silicon substrate, and is transmitted to the other pad from said input terminal via the other line.

This makes it possible to eliminate any branching of signal lines from an input pad to the input terminal on the silicon substrate, thereby making it possible to suppress any signal reflection arising from the branching of signal lines and to reduce the waveform distortion of the input signals of the source driver. As described above, with the drive circuit of this embodiment, the wiring of the data bus that supplies digital signals to the source drivers can be done easily by one-layer wiring, the branching of signal lines on the silicon substrate with the input pads of the respective source drivers can be eliminated, and waveform distortion of input signals arising from the branching of signal lines can be suppressed. In the above description, the drive circuit of an LCD panel was taken as an example, but the drive circuit of this invention is not limited to use for an LCD panel; needless to say, the principles of this invention can also be applied to other drive circuits that drive signal lines that have a large load with high-speed signals. In particular, the drive circuit of this invention is effective for supplying input signals from multiple signal lines to multiple drive elements.